



Europäisches Patentamt  
European Patent Office  
Office européen des brevets



Publication number: **0 366 263 A3**

**EUROPEAN PATENT APPLICATION**

Application number: 89309656.0

Int. Cl.<sup>5</sup>: **H04L 12/56**

Date of filing: 22.09.89

Priority: 25.10.88 GB 8824972

Date of publication of application:  
02.05.90 Bulletin 90/18

Designated Contracting States:  
BE DE ES FR GR IT LU NL SE

Date of deferred publication of the search report:  
16.09.92 Bulletin 92/38

Applicant: **GEC PLESSEY  
TELECOMMUNICATIONS LIMITED**  
New Century Park P.O. Box 53  
Coventry, CV3 1HJ(GB)

Inventor: **Proctor, Richard John**  
28 Diprose Road  
Corfe Mullen Wimborne Dorset(GB)  
Inventor: **Maddern, Thomas Slade**  
38 Cutlers Place  
Colehill Wimborne Dorset(GB)  
Inventor: **Philip, Alexander Schroder**  
31 Highland Road  
Wimborne Dorset(GB)

Representative: **Branfield, Henry Anthony**  
The General Electric Company plc Patent  
Department(Wembley Office) Hirst Research  
Centre East Lane  
Wembley, Middlesex HA9 7PP(GB)

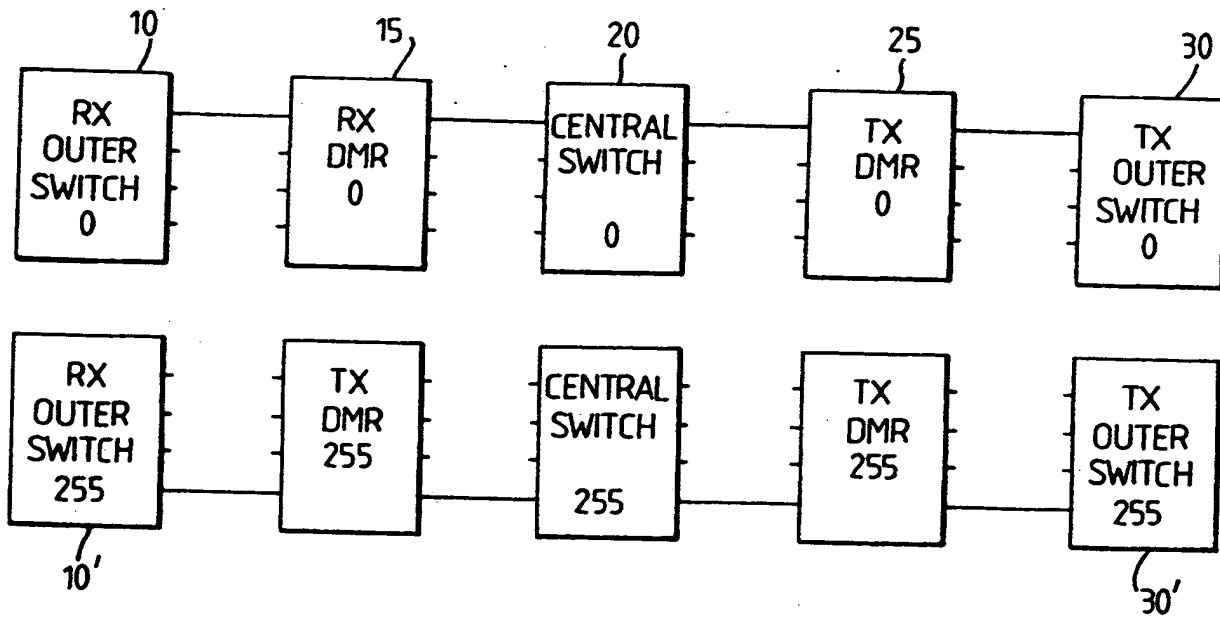
**Time division switch.**

The invention concerns Asynchronous Time Division Switches particularly for packet switching. In one embodiment a switch has 256 ports running at 155 M bits and is capable of switching incoming data cells at each of the input ports to any one of 256 output ports. At each input port a switch sequentially distributes the received data cells over 16 outputs each of which is connected to a different DMR circuit. There are 256 DMR circuits each having 16 inputs and 16 outputs. A DMR circuit is a fixed space switching device which has N inputs, N time intervals and N outputs and operates cyclically so that each input goes to each output for 1/Nth of the time. The inner stage of the ATD switch comprises 256 central switches each having 16 inputs and 16 outputs. Each central stage switch has its 16 inputs connected to 16 different DMR circuits. The fourth stage of the switch consists of another array

of 256 output DMR circuits with each central switch being connected to 16 different output DMR circuits. Each output DMR has its outputs connected to 16 different output ports. The internal circuitry of the ATD switch runs on 20 M bits. When a data cell is received at an input port its destination is derived from a header attached to the cell. Control circuitry enables the receiving port to request three address to query three possible routes through the switch. The ability to provide this series of questions is given by staggering the windows through which an output port can communicate with the central switches. Although data streams are received asynchronously the operation of the ATD switch is synchronous.

The switch is potentially capable of switching non ATD, synchronous traffic. Mixed mode of operation is possible.

*Fig.2.*





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number

EP 89 30 9656

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL5)
X	WO-A-8 807 298 (BELL TELEPHONE MANUFACTURING COMPANY) * abstract; claim 1 * * page 3, line 32 - page 4, line 23 * * page 5, line 7 - line 20 * * page 11, line 5 - line 10 *	1, 5-8	H04L12/56
A	---	2-4	
A	EP-A-0 274 793 (ALCATEL NV) * column 3, line 45 - column 4, line 48 *	2-4, 9, 10	
A	GLOBECOM 84 vol. 1, November 1984, ATLANTA, US pages 114 - 120; D. DIAS ET AL: 'PACKET SWITCHING IN N LOG N MULTISTAGE NETWORKS' * page 116, right column, line 10 - line 14 *	1	
P, X	EP-A-0 306 291 (BRITISH TELECOM) * claims 1-3 * * column 1, line 38 - line 40 * * column 1, line 41 - line 51 * * column 1, line 54 - line 60 * * column 2, line 1 - line 11 * * column 4, line 60 - column 5, line 5 * * column 6, line 33 - line 40 * * column 6, line 62 - column 7, line 8 *	1	
			TECHNICAL FIELDS SEARCHED (Int. CL5)
			H04L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 14 JULY 1992	Examiner ALI A.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

**THIS PAGE BLANK (USPTO)**